IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor integrated circuit device comprising:

a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated;

a first transmitter including a first serializer which converts parallel data into serial data synchronized with ~~one of~~ a transmit clock in a normal operation and a first test operation, and which converts the parallel data into the serial data synchronized with the clock generated by the first clock data recovery circuit in a second test operation;

a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated; and

a second transmitter including a second serializer which converts parallel data into serial data synchronized with ~~one of~~ a transmit clock in a normal operation and the second test operation, and which converts the parallel data into the serial data synchronized with the clock generated by the second clock data recovery circuit in the first test operation.

Claim 2 (Original): The device according to claim 1, wherein

the first and second transmitters are arranged between the first and second receivers, and

the first and second transmitters are adjacent to the first and second receivers, respectively.

Claim 3 (Original): The device according to claim 1, wherein

the first and second receivers are arranged between the first and second transmitters, and

the first and second receivers are adjacent to the first and second transmitters, respectively.

Claim 4 (Original): The device according to claim 2, further comprising:

a first loop-back path which loops serial data from the first transmitter back to the second receiver; and

a second loop-back path which loops serial data from the second transmitter back to the first receiver,

wherein the first and second loop-back paths are formed in a semiconductor integrated circuit device chip.

Claim 5 (Original): The device according to claim 3, further comprising:

a first loop-back path which loops serial data from the first transmitter back to the second receiver; and

a second loop-back path which loops serial data from the second transmitter back to the first receiver,

wherein the first and second loop-back paths are formed in a semiconductor integrated circuit device chip.

Claim 6 (Original): The device according to claim 1, wherein

the first and second transmitters are arranged between the first and second receivers, and

the first and second transmitters are adjacent to the second and first receivers, respectively.

Claim 7 (Original): The device according to claim 1, wherein

the first and second receivers are arranged between the first and second transmitters, and

the first and second receivers are adjacent to the second and first transmitters, respectively.

Claim 8 (Original): The device according to claim 4, further comprising:

a third loop-back path which loops serial data from the first transmitter back to the first receiver; and

a fourth loop-back path which loops serial data from the second transmitter back to the second receiver,

wherein the third and fourth loop-back paths are formed in the semiconductor integrated circuit device chip.

Claim 9 (Original): The device according to claim 5, further comprising:

a third loop-back path which loops serial data from the first transmitter back to the first receiver; and

a fourth loop-back path which loops serial data from the second transmitter back to the second receiver,

wherein the third and fourth loop-back paths are formed in the semiconductor integrated circuit device chip.

Claim 10 (Original): The device according to claim 6, further comprising:

a third loop-back path which loops serial data from the first transmitter back to the first receiver; and

a fourth loop-back path which loops serial data from the second transmitter back to the second receiver,

wherein the third and fourth loop-back paths are formed in the semiconductor integrated circuit device chip.

Claim 11 (Original): The device according to claim 7, further comprising:

a third loop-back path which loops serial data from the first transmitter back to the first receiver; and

a fourth loop-back path which loops serial data from the second transmitter back to the second receiver,

wherein the third and fourth loop-back paths are formed in the semiconductor integrated circuit device chip.

Claim 12 (Currently Amended): A semiconductor integrated circuit device comprising:

a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated on the basis of a frequency offset between the received serial data and a reference clock, or first phase control information for controlling a phase of a clock, and a first

deserializer which converts serial data synchronized with the generated clock into parallel data;

a first transmitter including a first serializer which converts parallel data into serial data synchronized with ~~one of~~ a transmit clock in a normal operation and a first test operation, and which converts the parallel data into the serial data synchronized with the clock generated by the first clock data recovery circuit in a second test operation;

a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated on the basis of a frequency offset between the received serial data and a reference clock, or second phase control information for controlling a phase of a clock, and a second deserializer which converts serial data synchronized with the generated clock into parallel data; and

a second transmitter including a second serializer which converts parallel data into serial data synchronized with ~~one of~~ a transmit clock in a normal operation and the second test operation, and which converts the parallel data into the serial data synchronized with the clock generated by the second clock data recovery circuit in the first test operation.

Claim 13 (Currently Amended): The device according to claim 12, wherein

~~when~~ in the second test operation, the second receiver is ~~to be~~ tested,

the first clock data recovery circuit changes a phase of a clock to be generated on the basis of the first phase control information, and outputs the phase-changed clock to the first transmitter,

the first transmitter transmits, to the second clock data recovery circuit, serial data synchronized with the phase-changed clock output from the first clock data recovery circuit, and

the second clock data recovery circuit receives the serial data transmitted from the first transmitter, and recovers the clock from the received serial data, and

~~when~~ in the first test operation, the first receiver is ~~to be~~ tested,

the second clock data recovery circuit changes a phase of a clock to be generated on the basis of the second phase control information, and outputs the phase-changed clock to the second transmitter,

the second transmitter transmits, to the first clock data recovery circuit, serial data synchronized with the phase-changed clock output from the second clock data recovery circuit, and

the first clock data recovery circuit receives the serial data transmitted from the second transmitter, and recovers the clock from the received serial data.

Claim 14 (Original): The device according to claim 12, further comprising:

a test control pattern generator; and

a test analyzer,

wherein the test control pattern generator generates the first and second phase control information, and

the test analyzer analyzes a state of the second clock data recovery circuit on the basis of the first phase control information and phase information of the clock recovered by the second clock data recovery circuit, and analyzes a state of the first clock data recovery circuit on the basis of the second phase control information and phase information of the clock recovered by the first clock data recovery circuit.

Claim 15 (Original): The device according to claim 14, wherein

the test control pattern generator comprises a first test control pattern generating circuit which generates the first phase control information, and a second test control pattern generating circuit which generates the second phase control information, and

the test analyzer comprises a first test analyzing circuit which analyzes the state of the first clock data recovery circuit, and a second test analyzing circuit which analyzes the state of the second clock data recovery circuit.

Claim 16 (Original): The device according to claim 12, wherein

the first and second transmitters are arranged between the first and second receivers, and

the first and second transmitters are adjacent to the first and second receivers, respectively.

Claim 17 (Original): The device according to claim 12, wherein

the first and second receivers are arranged between the first and second transmitters, and

the first and second receivers are adjacent to the first and second transmitters, respectively.

Claim 18 (Original): The device according to claim 12, wherein

the first and second transmitters are arranged between the first and second receivers, and

the first and second transmitters are adjacent to the second and first receivers, respectively.

Claim 19 (Original): The device according to claim 12, wherein

the first and second receivers are arranged between the first and second transmitters, and

the first and second receivers are adjacent to the second and first transmitters, respectively.

Claim 20 (Currently Amended): A test method for a semiconductor integrated circuit device ~~comprising~~ including a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated, a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the first clock data recovery circuit, a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated, and a second transmitter including a second serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the second clock data recovery circuit, the method comprising:

when testing the first receiver,

causing the second clock data recovery circuit to change a phase of a clock to be generated regardless of serial data, and to output the phase-changed clock to the second transmitter;

transmitting serial data synchronized with the phase-changed clock from the second transmitter to the first clock data recovery circuit;

causing the first clock data recovery circuit to receive the serial data transmitted from the second transmitter, and to recover the clock from the received serial data; and

analyzing a state of the first clock data recovery circuit on the basis of phase control information of the clock changed by the second clock data recovery circuit, and phase control information when the first clock data recovery circuit recovers the clock, and

when testing the second receiver[[,]]:

causing the first clock data recovery circuit to change a phase of a clock to be generated regardless of serial data, and to output the phase-changed clock to the first transmitter;

transmitting serial data synchronized with the phase-changed clock from the first transmitter to the second clock data recovery circuit;

causing the second clock data recovery circuit to receive the serial data transmitted from the first transmitter, and to recover the clock from the received serial data; and

analyzing a state of the second clock data recovery circuit on the basis of phase control information of the clock changed by the first clock data recovery circuit, and phase control information when the second clock data recovery circuit recovers the clock.